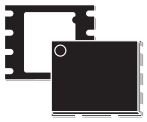
M25PE80

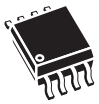
8 Mbit, low-voltage, Page-Erasable Serial Flash memory with Byte alterability, 50MHz SPI bus, standard pinout

Feature summary

- Industrial Standard SPI Pin-out
- 8 Mbits of Page-Erasable Flash Memory
- Page Write (up to 256 Bytes) in 11ms (typical)
- Page Program (up to 256 Bytes) in 1.35ms (typical)
- Page Erase (256 Bytes) in 10ms (typical)
- Sector Erase (512 Kbits)
- Bulk Erase (8 Mbits)
- 2.7 to 3.6V Single Supply Voltage
- SPI Bus Compatible Serial Interface
- 50MHz Clock Rate (maximum)
- Deep Power-down Mode 1µA (typical)
- Electronic Signature
  - JEDEC Standard Two-Byte Signature (8014h)
- More than 100,000 Write Cycles
- More than 20 Year Data Retention
- Hardware Write Protection of the Top Sector (64KB)
- Software Write Protection on a 64KByte Sector Basis
- Software Write Protection on a 4KByte Sub-sector Basis for Sector 0 and Sector 15
- Packages
  - ECOPACK® (RoHS compliant)



VFQFPN8 (MP)
6 x 5mm (MLP8)



SO8W (MW)
208 mils width

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1 Summary description

The M25PE80 is an 8 Mbit (1Mb x 8) Serial Paged Flash Memory accessed by a high speed SPI-compatible bus.

The memory can be written or programmed 1 to 256 Bytes at a time, using the Page Write or Page Program instruction. The Page Write instruction consists of an integrated Page Erase cycle followed by a Page Program cycle.

The memory is organized as 16 sectors, each containing 256 pages. Each page is 256 Bytes wide. Thus, the whole memory can be viewed as consisting of 4096 pages, or 1,048,576 Bytes.

The memory can be erased a page at a time, using the Page Erase instruction, a sector at a time, using the Sector Erase instruction, or as a whole, using the Bulk Erase instruction.

The memory can be Write Protected by either Hardware or Software, with a protection granularity of either 64 KBytes (sector granularity) or 4 KBytes (sub-sector granularity inside sector 0 and sector 15 only).

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages.
ECOPACK® packages are Lead-free and RoHS compliant.

ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*.

Figure 1. Logic diagram

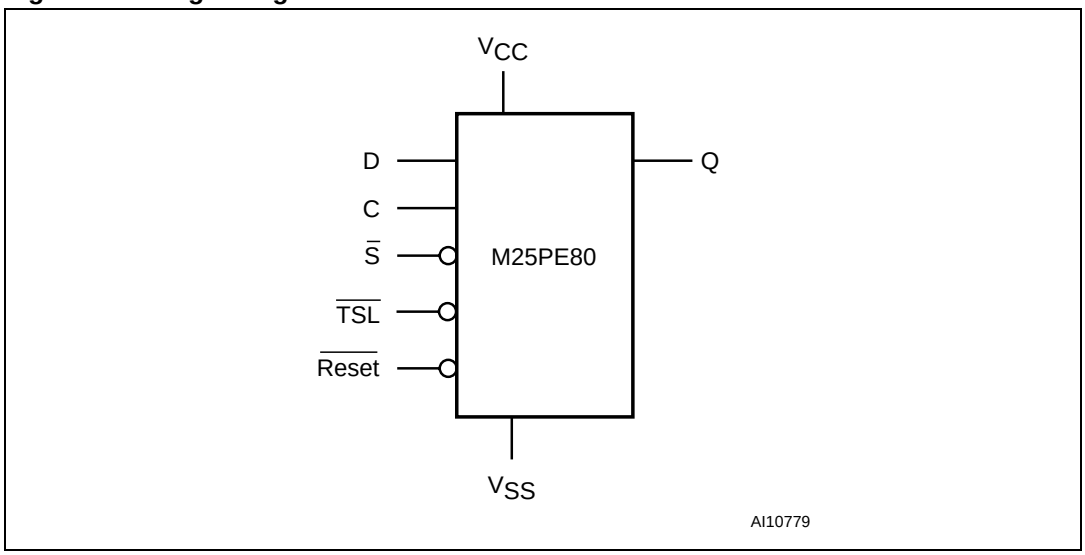
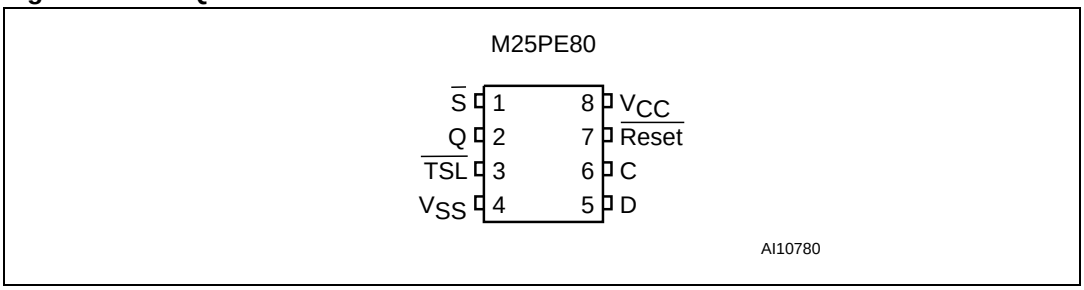


Table 1. Signal names

C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
$\overline{S}$	Chip Select
$\overline{TSL}$	Top Sector Lock
$\overline{Reset}$	Reset
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2. VFQFPN and SO connections



1. There is an exposed die paddle on the underside of the MLP8 package. This is pulled, internally, to V_{SS}, and must not be allowed to be connected to any other voltage or signal line on the PCB.
2. See *Package mechanical* section for package dimensions, and how to identify pin-1.

2 Signal description

2.1 Serial Data Output (Q)

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (C).

2.2 Serial Data Input (D)

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be programmed. Values are latched on the rising edge of Serial Clock (C).

2.3 Serial Clock (C)

This input signal provides the timing of the serial interface. Instructions, addresses, or data present at Serial Data Input (D) are latched on the rising edge of Serial Clock (C). Data on Serial Data Output (Q) changes after the falling edge of Serial Clock (C).

2.4 Chip Select ($\overline{S}$)

When this input signal is High, the device is deselected and Serial Data Output (Q) is at high impedance. Unless an internal Read, Program, Erase or Write cycle is in progress, the device will be in the Standby mode (this is not the Deep Power-down mode). Driving Chip Select ($\overline{S}$) Low selects the device, placing it in the Active Power mode.

After Power-up, a falling edge on Chip Select ($\overline{S}$) is required prior to the start of any instruction.

2.5 Reset ($\overline{Reset}$)

The Reset ($\overline{Reset}$) input provides a hardware reset for the memory.

When Reset ($\overline{Reset}$) is driven High, the memory is in the normal operating mode. When Reset ($\overline{Reset}$) is driven Low, the memory will enter the Reset mode. In this mode, the output is high impedance.

Driving Reset ($\overline{Reset}$) Low while an internal operation is in progress will affect this operation (write, program or erase cycle) and data may be lost.

2.6 Top Sector Lock ($\overline{TSL}$)

This input signal puts the device in the Hardware Protected mode, when Top Sector Lock ($\overline{TSL}$) is connected to V_{SS}, causing the top 256 pages (upper addresses) of the memory to become read-only (protected from write, program and erase operations).

When Top Sector Lock ($\overline{TSL}$) is connected to V_{CC}, the top 256 pages of memory behave like the other pages of memory.

3 SPI modes

These devices can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:

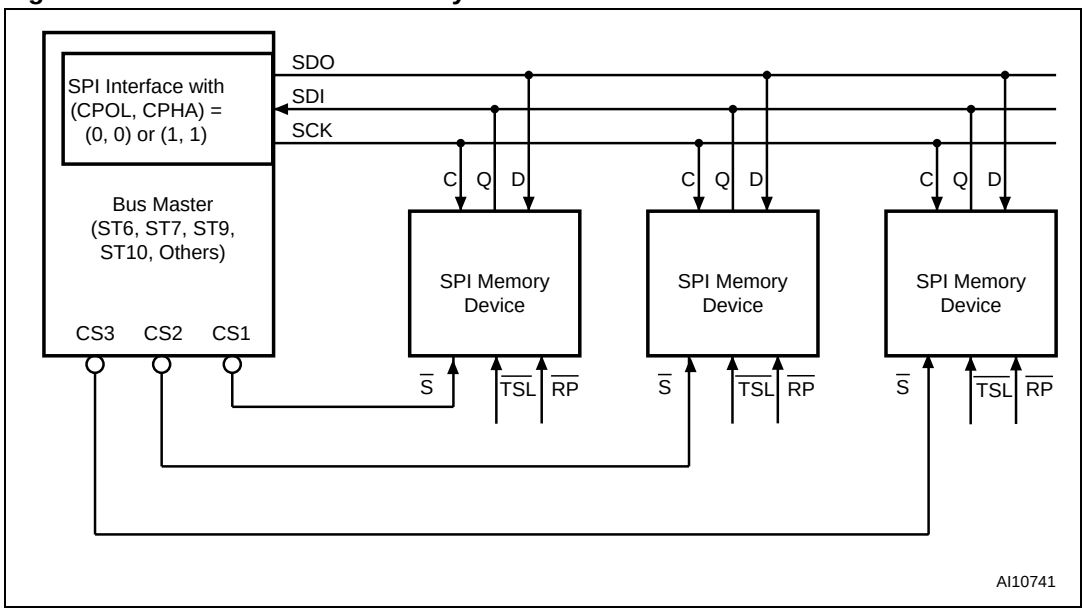
- CPOL=0, CPHA=0
- CPOL=1, CPHA=1

For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

The difference between the two modes, as shown in *Figure 4*, is the clock polarity when the bus master is in Stand-by mode and not transferring data:

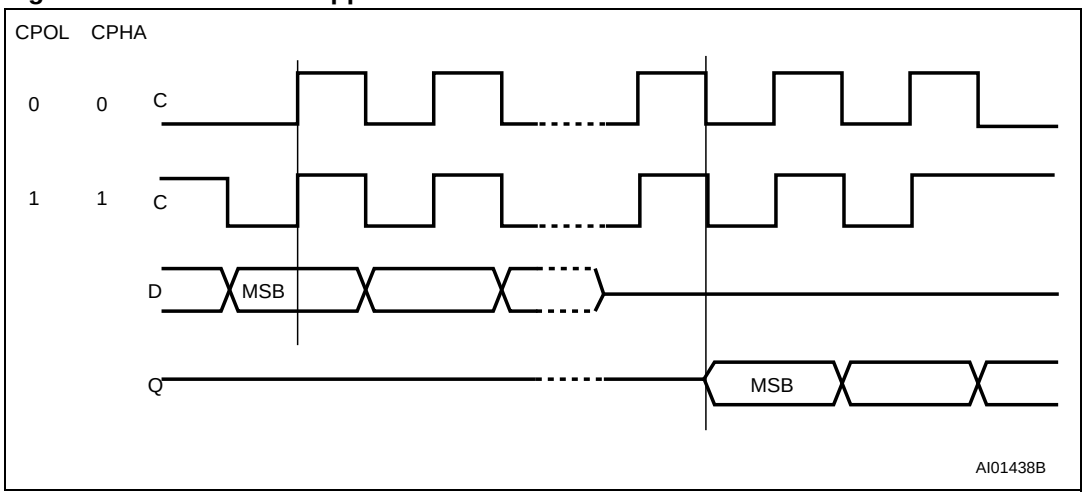
- C remains at 0 for (CPOL=0, CPHA=0)
- C remains at 1 for (CPOL=1, CPHA=1)

Figure 3. Bus master and memory devices on the SPI bus



1. The Top Sector Lock ($\overline{TSL}$) signal should be driven, High or Low as appropriate.

Figure 4. SPI modes supported



4 Operating features

4.1 Sharing the overhead of modifying data

To write or program one (or more) data Bytes, two instructions are required: Write Enable (WREN), which is one Byte, and a Page Write (PW) or Page Program (PP) sequence, which consists of four Bytes plus data. This is followed by the internal cycle (of duration t_{PW} or t_{PP}).

To share this overhead, the Page Write (PW) or Page Program (PP) instruction allows up to 256 Bytes to be programmed (changing bits from 1 to 0) or written (changing bits to 0 or 1) at a time, provided that they lie in consecutive addresses on the same page of memory.

4.2 An easy way to modify data

The Page Write (PW) instruction provides a convenient way of modifying data (up to 256 contiguous Bytes at a time), and simply requires the start address, and the new data in the instruction sequence.

The Page Write (PW) instruction is entered by driving Chip Select ($\overline{S}$) Low, and then transmitting the instruction Byte, three address Bytes (A23-A0) and at least one data Byte, and then driving Chip Select ($\overline{S}$) High. While Chip Select ($\overline{S}$) is being held Low, the data Bytes are written to the data buffer, starting at the address given in the third address Byte (A7-A0). When Chip Select ($\overline{S}$) is driven High, the Write cycle starts. The remaining, unchanged, Bytes of the data buffer are automatically loaded with the values of the corresponding Bytes of the addressed memory page. The addressed memory page then automatically put into an Erase cycle. Finally, the addressed memory page is programmed with the contents of the data buffer.

All of this buffer management is handled internally, and is transparent to the user. The user is given the facility of being able to alter the contents of the memory on a Byte-by-Byte basis.

For optimized timings, it is recommended to use the Page Write (PW) instruction to write all consecutive targeted Bytes in a single sequence versus using several Page Write (PW) sequences with each containing only a few Bytes (see *Page Write (PW)* section and <Blue>Table 16., AC Characteristics).

4.3 A fast way to modify data

The Page Program (PP) instruction provides a fast way of modifying data (up to 256 contiguous Bytes at a time), provided that it only involves resetting bits to 0 that had previously been set to 1.

This might be:

- when the designer is programming the device for the first time
- when the designer knows that the page has already been erased by an earlier Page Erase (PE), Sector Erase (SE) or Bulk Erase (BE) instruction. This is useful, for example, when storing a fast stream of data, having first performed the erase cycle when time was available
- when the designer knows that the only changes involve resetting bits to 0 that are still set to 1. When this method is possible, it has the additional advantage of minimising the number of unnecessary erase operations, and the extra stress incurred by each page

For optimized timings, it is recommended to use the Page Program (PP) instruction to program all consecutive targeted Bytes in a single sequence versus using several Page Program (PP) sequences with each containing only a few Bytes (see *Page Program (PP)* section and *Table 16: AC Characteristics*).

4.4 Polling during a Write, Program or Erase cycle

A further improvement in the write, program or erase time can be achieved by not waiting for the worst case delay (t_{PW}, t_{PP}, t_{PE}, t_{SE} or t_{BE}). The Write In Progress (WIP) bit is provided in the Status Register so that the application program can monitor its value, polling it to establish when the previous cycle is complete.

4.5 Reset

An internal Power-On Reset circuit helps protect against inadvertent data writes. Addition protection is provided by driving Reset ($\overline{\text{RESET}}$) Low during the Power-on process, and only driving it High when V_{CC} has reached the correct voltage level, V_{CC}(min).

4.6 Active Power, Standby Power and Deep Power-Down modes

When Chip Select ($\overline{S}$) is Low, the device is selected, and in the Active Power mode.

When Chip Select ($\overline{S}$) is High, the device is deselected, but could remain in the Active Power mode until all internal cycles have completed (Program, Erase, Write). The device then goes in to the Standby Power mode. The device consumption drops to I_{CC1}.

The Deep Power-down mode is entered when the specific instruction (the Deep Power-down (DP) instruction) is executed. The device consumption drops further to I_{CC2}. When in this mode, only the Release from Deep Power-down instruction is accepted. All other instructions are ignored. The device remains in the Deep Power-down mode until the Release from Deep Power-down instruction is executed. This can be used as an extra software protection mechanism, when the device is not in active use, to protect the device from inadvertent Write, Program or Erase instructions.

4.7 Status Register

The Status Register contains two status bits that can be read by the Read Status Register (RDSR) instruction. See *Section 6.4: Read Status Register (RDSR)* for a detailed description of the Status Register bits.

4.8 Protection modes

The environments where non-volatile memory devices are used can be very noisy. No SPI device can operate correctly in the presence of excessive noise. To help combat this, the M25PE80 features the following data protection mechanisms:

- Power On Reset and an internal timer (t_{PUW}) can provide protection against inadvertant changes while the power supply is outside the operating specification.
- Program, Erase and Write instructions are checked that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution.
- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit. This bit is returned to its reset state by the following events:
  - Power-up
  - Reset ($\overline{\text{RESET}}$) driven Low
  - Write Disable (WRDI) instruction completion
  - Page Write (PW) instruction completion
  - Page Program (PP) instruction completion
  - Write to Lock Register (WRLR) instruction completion
  - Page Erase (PE) instruction completion
  - Sector Erase (SE) instruction completion
  - Bulk Erase (BE) instruction completion
- The Hardware Protected mode is entered when Top Sector Lock ($\overline{\text{TSL}}$) is driven Low, causing the top 256 pages of memory to become read-only. When Top Sector Lock ($\overline{\text{TSL}}$) is driven High, the top 256 pages of memory behave like the other pages of memory.
- The Reset ($\overline{\text{Reset}}$) signal can be driven Low to protect the contents of the memory during any critical time, not just during Power-up and Power-down.
- In addition to the low power consumption feature, the Deep Power-down mode offers extra software protection from inadvertant Write, Program and Erase instructions while the device is not in active use.
- The Software Protection is managed by specific Lock Registers assigned to each sector and sub-sector as follows:
  - Each 64KB sector has a Lock Register.
  - Inside sector 0 and sector 15, each 4KB sub-sector also has a Lock Register (in addition to the Lock Register at sector level).

  The Lock Registers can be read and written using the Read Lock Register (RDLR) and Write to Lock Register (WRLR) instructions.

  In each Lock Register two bits control the protection of each sector/sub-sector: the Write Lock Bit and the Lock Down Bit.

– Write Lock Bit:

The Write Lock Bit determines whether the contents of the sector/sub-sector can be modified (using the Write, Program or Erase instructions). When the Write Lock Bit is set, '1', the sector/sub-sector is write protected – any operations that attempt to change the data in the sector/sub-sector will fail. When the Write Lock Bit is reset to '0', the sector/sub-sector is not write protected by the Lock Register, and may be modified, unless $\overline{TSL}$ is Low (in which case the top sector will remain write protected).

– Lock Down Bit:

The Lock Down Bit provides a mechanism for protecting software data from simple hacking and malicious attack. When the Lock Down Bit is set, '1', further modification to the Write Lock and Lock Down Bits cannot be performed. A reset, or power-up, is required before changes to these bits can be made. When the Lock Down Bit is reset, '0', the Write Lock and Lock Down Bits can be changed.

The Write Lock Bit and the Lock Down Bit are volatile and their value is reset to '0' after a Power-Down or a Reset.

The definition of the Lock Register bits is given in *Table 8: Lock Register Out*.

Refer to *Table 2* and *Table 3* for details on the Software Protection for sectors 1 to 14 and 0 and 15, respectively. *Figure 5* shows the the Software Protection scheme.

Table 2. Software protection truth table (Sectors 1 to 14)

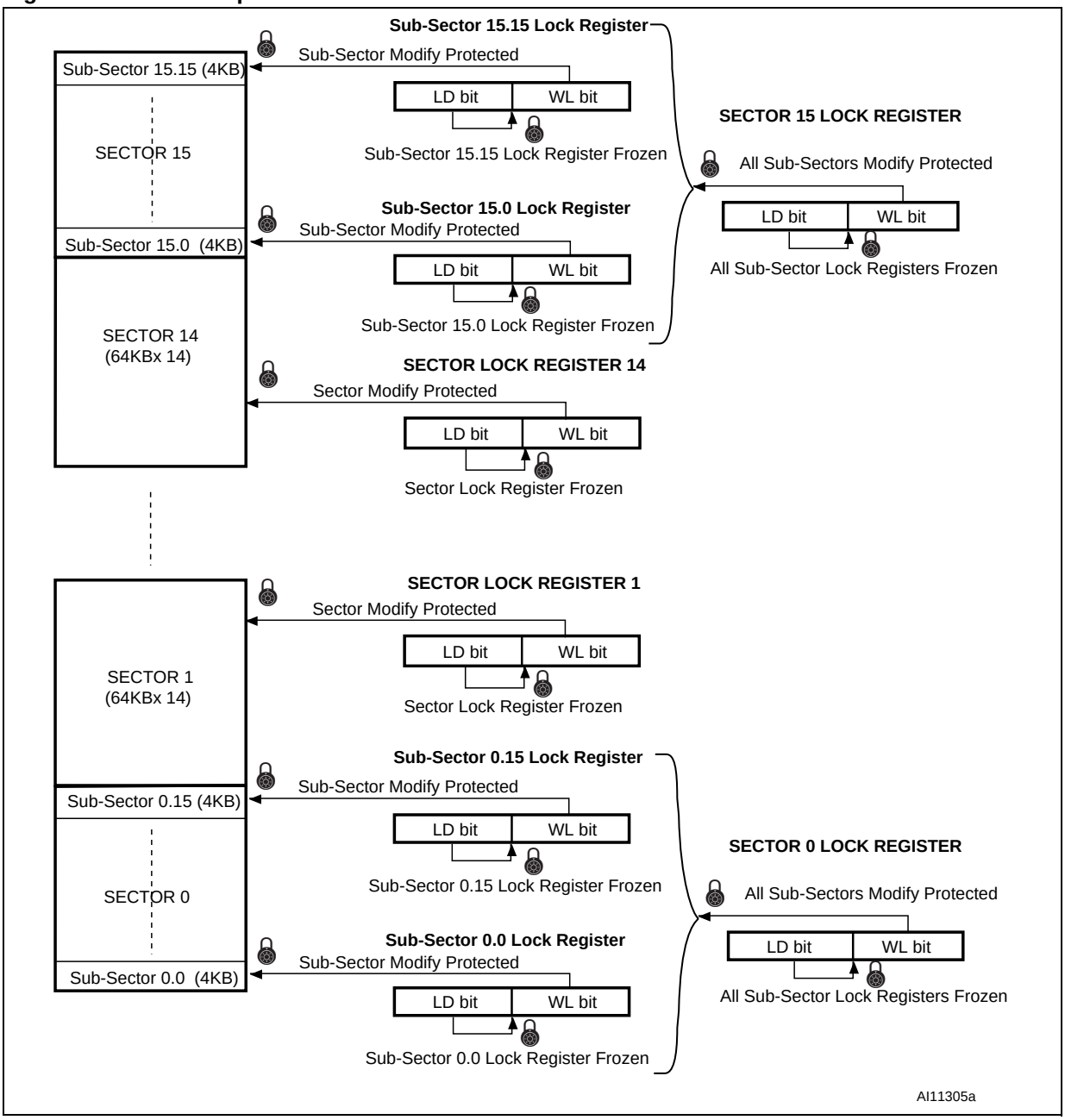
Sector Lock Register		Protection Status
Lock Down Bit	Write Lock Bit	
0	0	Sector Unprotected from Program/Erase/Write operations, Protection Status Reversible
0	1	Sector Protected from Program/Erase/Write operations, Protection Status Reversible
1	0	Sector Unprotected from Program/Erase/Write operations, Sector Protection Status cannot be changed except by a Reset or Power-up.
1	1	Sector Protected from Program/Erase/Write operations, Sector Protection Status cannot be changed except by a Reset or Power-up.

Table 3. Software protection scheme truth table (Sectors 0 and 15)(1) (2)

Sector Lock Register		Sub-Sector Lock Register		Protection Status
Lock Down Bit	Write Lock Bit	Lock Down Bit	Write Lock Bit	
0	0	0	0	Current Sub-Sector Unprotected from Program/Erase/Write operations, Current Sub-Sector Protection Status Reversible
		0	1	Current Sub-Sector Protected from Program/Erase/Write operations, Current Sub-Sector Protection Status Reversible.
		1	0	Current Sub-Sector Unprotected from Program/Erase/Write operations, Current Sub-Sector Protection Status cannot be changed except by a Reset or Power-up.
		1	1	Current Sub-Sector Protected from Program/Erase/Write operations, Current Sub-Sector Protection Status cannot be changed except by a Reset or Power-up.
	1	0	1	All Sub-Sectors Protected from Program/Erase/Write operations, Current Sub-Sector Protection Status Reversible
		1	1	All Sub-Sectors Protected from Program/Erase/Write operations, Current Sub-sector Protection Status cannot be changed except by a Reset or Power-up.
1	0	1	0	Current Sub-Sector Unprotected from Program/Erase/Write operations, All Sub-sectors Protection Status cannot be changed except by a Reset or Power-up
		1	1	Current Sub-Sector Protected from Program/Erase/Write operations, All Sub-sectors Protection Status cannot be changed except by a Reset or Power-up
	1	1	1	All Sub-sectors Protected with their Protection Status cannot be changed except by a Reset or Power-up.

1. All other bit combinations are not-applicable.
2. For more details, refer to the description of the *Write to Lock Register (WRLR)* instruction.

Figure 5. Software protection scheme



1. LD Lock Down bit; WL Write Lock bit.

5 Memory organization

The memory is organized as:

- 4096 pages (256 Bytes each).
- 1,048,576 Bytes (8 bits each)
- 16 sectors (512 Kbits, 65536 Bytes each)

Each page can be individually:

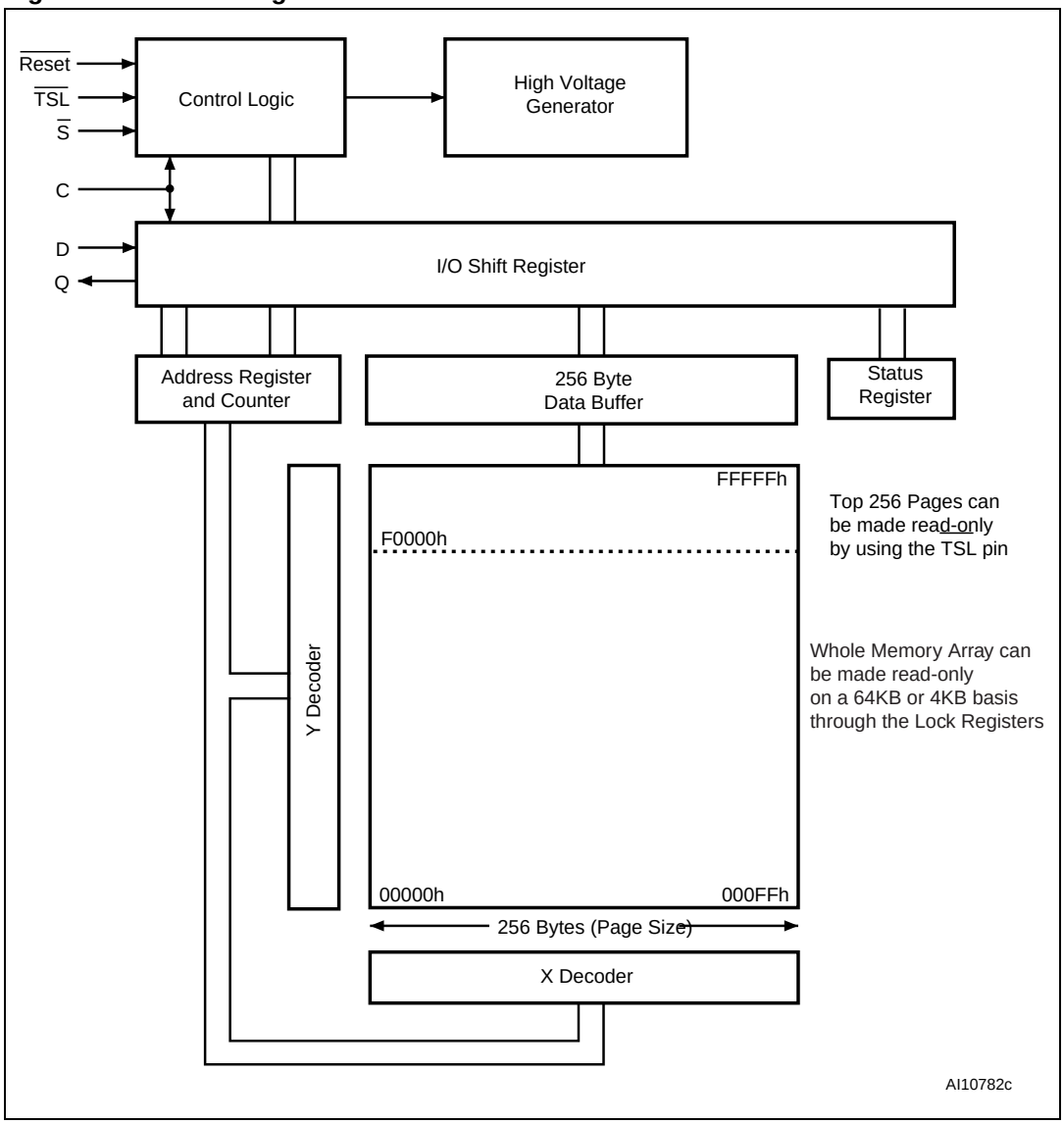
- programmed (bits are programmed from 1 to 0)
- erased (bits are erased from 0 to 1)
- written (bits are changed to either 0 or 1)

The device is Page, Sector or Bulk Erasable (bits are erased from 0 to 1).

Table 4. Memory organization

Sector	Address Range	
15	F0000h	FFFFFh
14	E0000h	EFFFFh
13	D0000h	DFFFFh
12	C0000h	CFFFFh
11	B0000h	BFFFFh
10	A0000h	AFFFFh
9	90000h	9FFFFh
8	80000h	8FFFFh
7	70000h	7FFFFh
6	60000h	6FFFFh
5	50000h	5FFFFh
4	40000h	4FFFFh
3	30000h	3FFFFh
2	20000h	2FFFFh
1	10000h	1FFFFh
0	00000h	0FFFFh

Figure 6. Block Diagram



6 Instructions

All instructions, addresses and data are shifted in and out of the device, most significant bit first.

Serial Data Input (D) is sampled on the first rising edge of Serial Clock (C) after Chip Select ($\overline{S}$) is driven Low. Then, the one-Byte instruction code must be shifted in to the device, most significant bit first, on Serial Data Input (D), each bit being latched on the rising edges of Serial Clock (C).

The instruction set is listed in *Table 5*.

Every instruction sequence starts with a one-Byte instruction code. Depending on the instruction, this might be followed by address Bytes, or by data Bytes, or by both or none.

In the case of a Read Data Bytes (READ), Read Data Bytes at Higher Speed (Fast_Read), Read Identification (RDID), Read Status Register (RDSR), or Read Lock Register (RDLR) instruction, the shifted-in instruction sequence is followed by a data-out sequence. Chip Select ($\overline{S}$) can be driven High after any bit of the data-out sequence is being shifted out.

In the case of a Page Write (PW), Page Program (PP), Write to Lock Register (WRLR), Page Erase (PE), Sector Erase (SE), Bulk Erase (BE), Write Enable (WREN), Write Disable (WRDI), Deep Power-down (DP) or Release from Deep Power-down (RDP) instruction, Chip Select ($\overline{S}$) must be driven High exactly at a Byte boundary, otherwise the instruction is rejected, and is not executed. That is, Chip Select ($\overline{S}$) must driven High when the number of clock pulses after Chip Select ($\overline{S}$) being driven Low is an exact multiple of eight.

All attempts to access the memory array during a Write cycle, Program cycle or Erase cycle are ignored, and the internal Write cycle, Program cycle or Erase cycle continues unaffected.

Table 5. Instruction set

Instruction	Description	One-Byte Instruction Code		Address Bytes	Dummy Bytes	Data Bytes
WREN	Write Enable	0000 0110	06h	0	0	0
WRDI	Write Disable	0000 0100	04h	0	0	0
RDID	Read Identification	1001 1111	9Fh	0	0	1 to 3
RDSR	Read Status Register	0000 0101	05h	0	0	1 to ∞
WRLR	Write to Lock Register	1110 0101	E5h	3	0	1
RDLR	Read Lock Register	1110 1000	E8h	3	0	1
READ	Read Data Bytes	0000 0011	03h	3	0	1 to ∞
FAST_READ	Read Data Bytes at Higher Speed	0000 1011	0Bh	3	1	1 to ∞
PW	Page Write	0000 1010	0Ah	3	0	1 to 256
PP	Page Program	0000 0010	02h	3	0	1 to 256
PE	Page Erase	1101 1011	DBh	3	0	0
SE	Sector Erase	1101 1000	D8h	3	0	0
BE	Bulk Erase	1100 0111	C7h	0	0	0
DP	Deep Power-down	1011 1001	B9h	0	0	0
RDP	Release from Deep Power-down	1010 1011	ABh	0	0	0

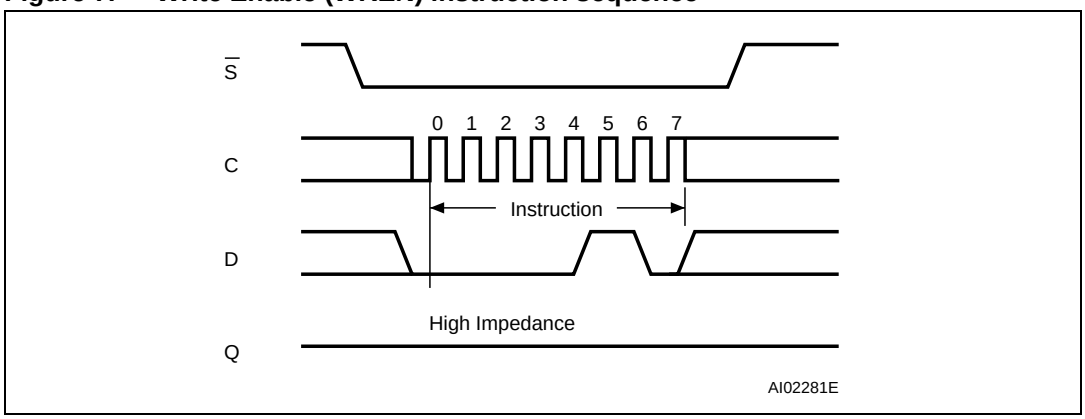
6.1 Write Enable (WREN)

The Write Enable (WREN) instruction (*Figure 7*) sets the Write Enable Latch (WEL) bit.

The Write Enable Latch (WEL) bit must be set prior to every Page Write (PW), Page Program (PP), Page Erase (PE), Sector Erase (SE), Bulk Erase (BE) and Write to Lock Register (WRLR) instructions.

The Write Enable (WREN) instruction is entered by driving Chip Select ($\overline{S}$) Low, sending the instruction code, and then driving Chip Select ($\overline{S}$) High.

Figure 7. Write Enable (WREN) instruction sequence



6.2 Write Disable (WRDI)

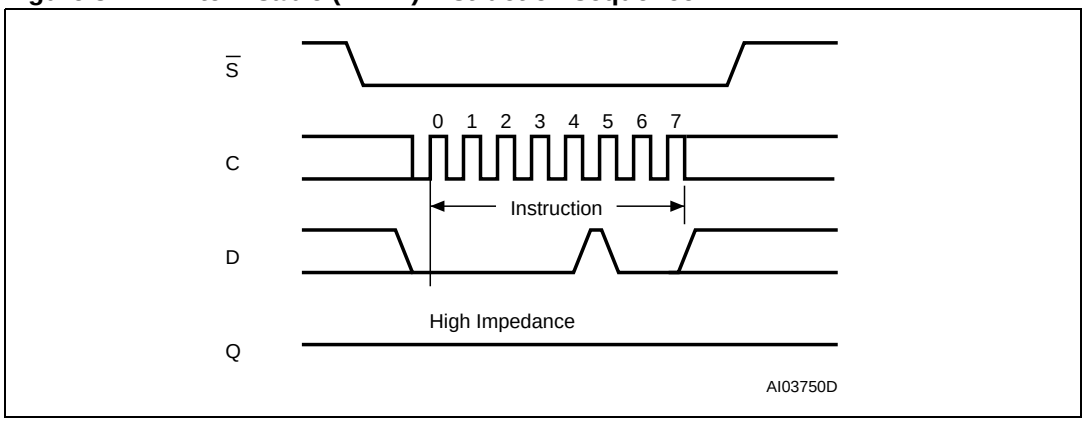
The Write Disable (WRDI) instruction (*Figure 8*) resets the Write Enable Latch (WEL) bit.

The Write Disable (WRDI) instruction is entered by driving Chip Select ($\overline{S}$) Low, sending the instruction code, and then driving Chip Select ($\overline{S}$) High.

The Write Enable Latch (WEL) bit is reset under the following conditions:

- Power-up
- Write Disable (WRDI) instruction completion
- Page Write (PW) instruction completion
- Page Program (PP) instruction completion
- Write to Lock Register (WRLR) instruction completion
- Page Erase (PE) instruction completion
- Sector Erase (SE) instruction completion
- Bulk Erase (BE) instruction completion

Figure 8. Write Disable (WRDI) instruction sequence



6.3 Read Identification (RDID)

The Read Identification (RDID) instruction allows the 8-bit manufacturer identification to be read, followed by two Bytes of device identification. The manufacturer identification is assigned by JEDEC, and has the value 20h for STMicroelectronics. The device identification is assigned by the device manufacturer, and indicates the memory type in the first Byte (80h), and the memory capacity of the device in the second Byte (14h).

Any Read Identification (RDID) instruction while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress.

The device is first selected by driving Chip Select ($\overline{S}$) Low. Then, the 8-bit instruction code for the instruction is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output (Q), each bit being shifted out during the falling edge of Serial Clock (C).

The instruction sequence is shown in *Figure 9*.

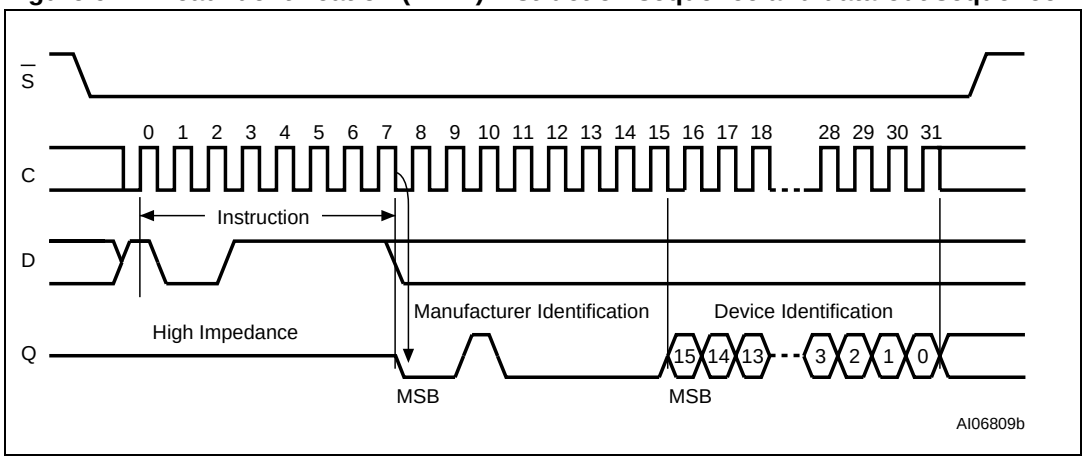
The Read Identification (RDID) instruction is terminated by driving Chip Select ($\overline{S}$) High at any time during data output.

When Chip Select ($\overline{S}$) is driven High, the device is put in the Stand-by Power mode. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

Table 6. Read Identification (RDID) data-out sequence

Manufacturer Identification	Device Identification	
	Memory Type	Memory Capacity
20h	80h	14h

Figure 9. Read Identification (RDID) instruction sequence and data-out sequence



6.4 Read Status Register (RDSR)

The Read Status Register (RDSR) instruction allows the Status Register to be read. The Status Register may be read at any time, even while a Program, Erase or Write cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously, as shown in *Figure 10*.

The status bits of the Status Register are as follows:

6.4.1 WIP bit

The Write In Progress (WIP) bit indicates whether the memory is busy with a Write, Program or Erase cycle. When set to 1, such a cycle is in progress, when reset to 0 no such cycle is in progress.

6.4.2 WEL bit

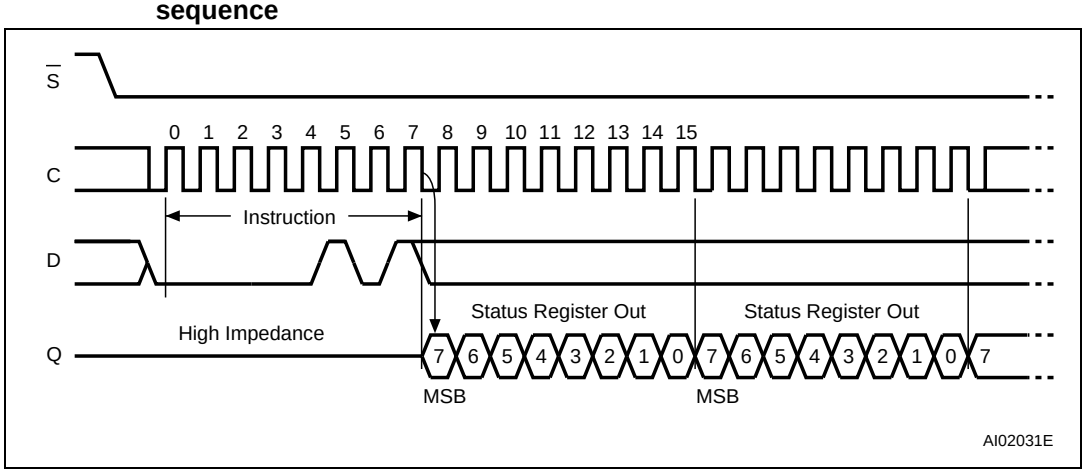
The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write, Program or Erase instruction is accepted.

Table 7. Status Register format

b7							b0
0	0	0	0	0	0	WEL(1)	WIP(1)

1. WEL and WIP are volatile read-only bits (WEL is set and reset by specific instructions; WIP is automatically set and reset by the internal logic of the device).

Figure 10. Read Status Register (RDSR) instruction sequence and data-out sequence



6.5 Read Data Bytes (READ)

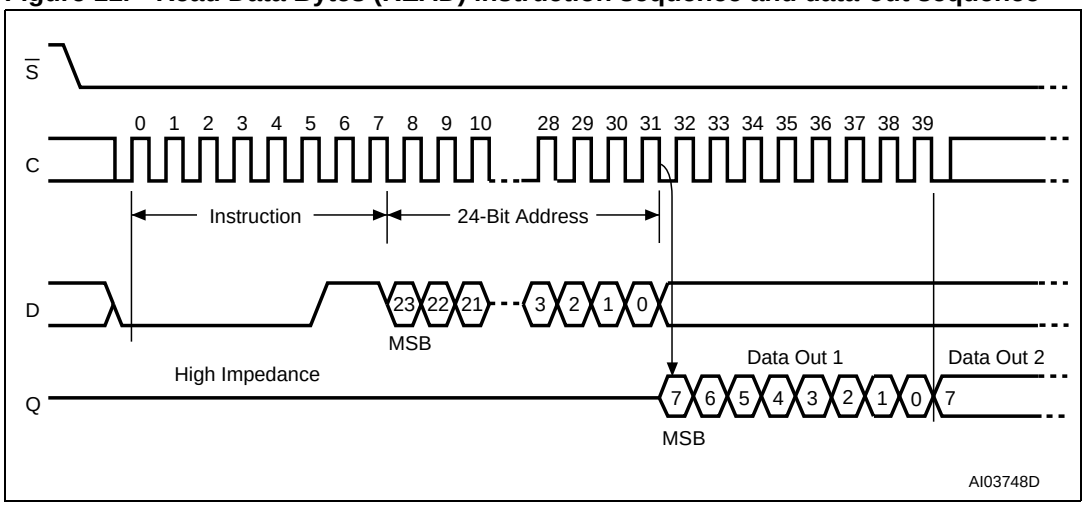
The device is first selected by driving Chip Select ($\overline{S}$) Low. The instruction code for the Read Data Bytes (READ) instruction is followed by a 3-Byte address (A23-A0), each bit being latched-in during the rising edge of Serial Clock (C). Then the memory contents, at that address, is shifted out on Serial Data Output (Q), each bit being shifted out, at a maximum frequency f_R, during the falling edge of Serial Clock (C).

The instruction sequence is shown in *Figure 11*.

The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each Byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The Read Data Bytes (READ) instruction is terminated by driving Chip Select ($\overline{S}$) High. Chip Select ($\overline{S}$) can be driven High at any time during data output. Any Read Data Bytes (READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 11. Read Data Bytes (READ) instruction sequence and data-out sequence



1. Address bits A23 to A20 are Don't Care.

6.6 Read Data Bytes at Higher Speed (FAST_READ)

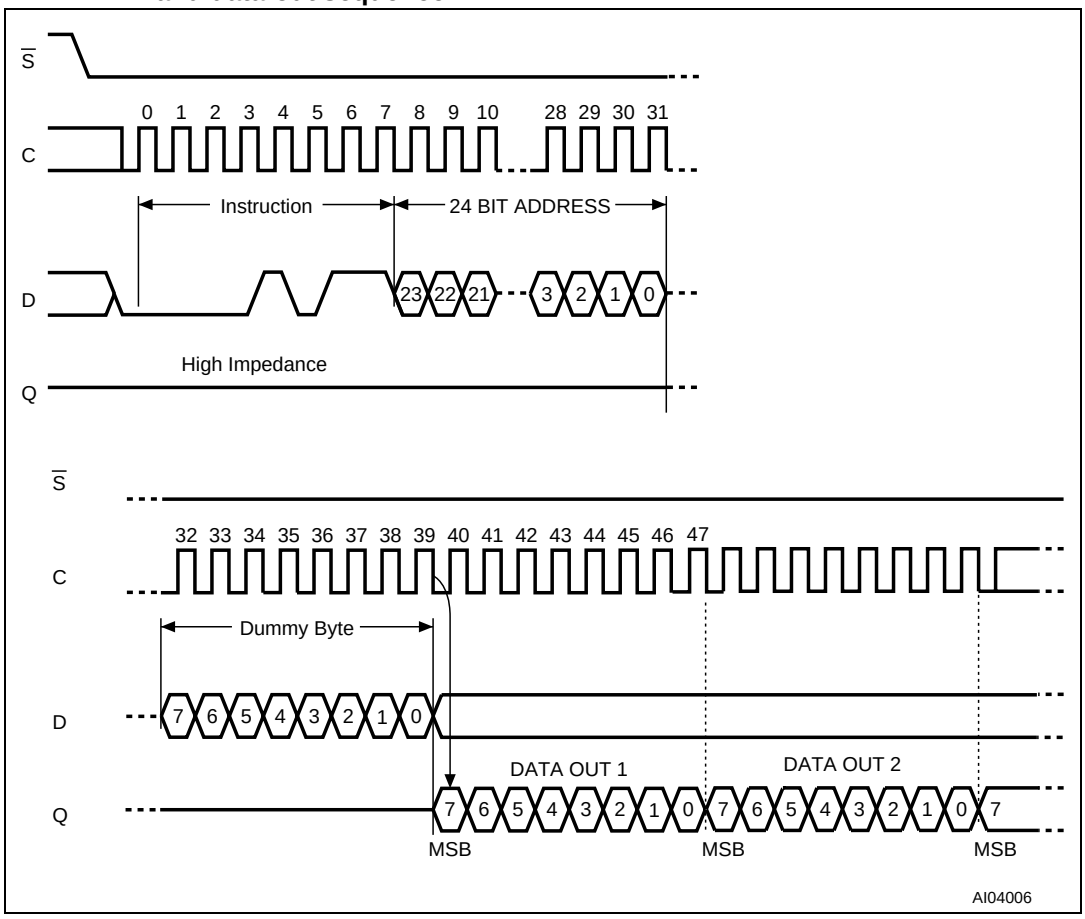
The device is first selected by driving Chip Select ($\overline{S}$) Low. The instruction code for the Read Data Bytes at Higher Speed (FAST_READ) instruction is followed by a 3-Byte address (A23-A0) and a dummy Byte, each bit being latched-in during the rising edge of Serial Clock (C). Then the memory contents, at that address, is shifted out on Serial Data Output (Q), each bit being shifted out, at a maximum frequency f_C, during the falling edge of Serial Clock (C).

The instruction sequence is shown in *Figure 12*.

The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each Byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes at Higher Speed (FAST_READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The Read Data Bytes at Higher Speed (FAST_READ) instruction is terminated by driving Chip Select ($\overline{S}$) High. Chip Select ($\overline{S}$) can be driven High at any time during data output. Any Read Data Bytes at Higher Speed (FAST_READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 12. Read Data Bytes at Higher Speed (FAST_READ) instruction sequence and data-out sequence



1. Address bits A23 to A20 are Don't Care.

6.7 Read Lock Register (RDLR)

The device is first selected by driving Chip Select ($\overline{S}$) Low. The instruction code for the Read Lock Register (RDLR) instruction is followed by a 3-Byte address (A23-A0) pointing to any location inside the concerned sector (or sub-sector). Each address bit is latched-in during the rising edge of Serial Clock (C). Then the value of the Lock Register is shifted out on Serial Data Output (Q), each bit being shifted out, at a maximum frequency f_C, during the falling edge of Serial Clock (C).

The instruction sequence is shown in *Figure 13*.

The Read Lock Register (RDLR) instruction is terminated by driving Chip Select ($\overline{S}$) High at any time during data output.

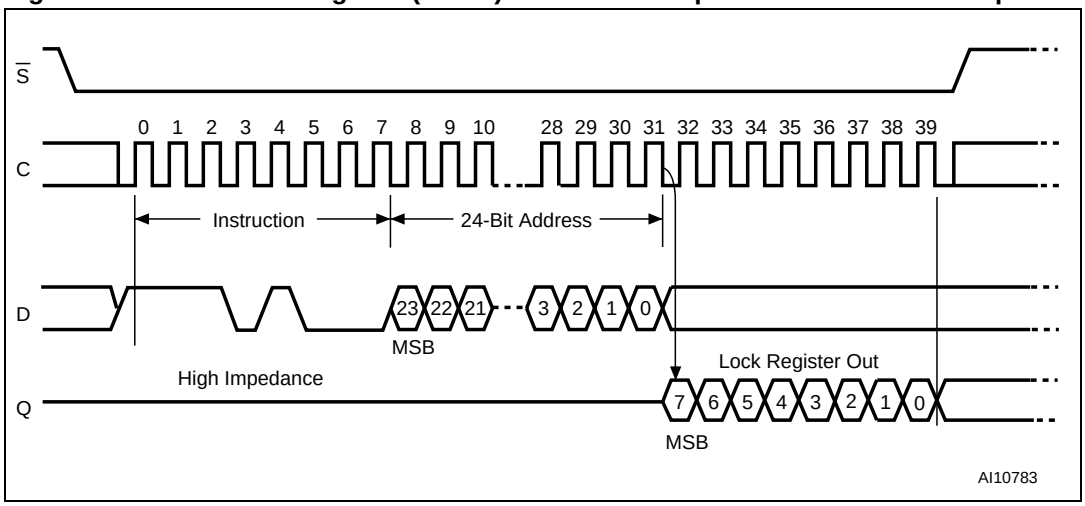
Any Read Lock Register (RDLR) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Table 8. Lock Register Out

Bit	Bit Name	Value	Function
b7-b4	Reserved		
b3	Sub-sector Lock Down(1)	‘1’	The Write Lock and Lock Down Bits cannot be changed Once a ‘1’ is written to the Lock Down Bit it cannot be cleared to ‘0’ except by a Reset or power-up.
		‘0’	The Write Lock and Lock Down Bits can be changed by writing new values to them. (Default value).
b2	Sub-sector Write Lock(1)	‘1’	Write, Program and Erase operations in this sub-sector will not be executed. The memory contents will not be changed.
		‘0’	Write, Program and Erase operations in this sub-sector are executed and will modify the sub-sector contents. (Default value).
b1	Sector Lock Down	‘1’	The Write Lock and Lock Down Bits cannot be changed. Once a ‘1’ is written to the Lock Down Bit it cannot be cleared to ‘0’, except by a Reset or power-up.
		‘0’	The Write Lock and Lock Down Bits can be changed by writing new values to them. (Default value).
b0	Sector Write Lock	‘1’	Write, Program and Erase operations in this sector will not be executed. The memory contents will not be changed.
		‘0’	Write, Program and Erase operations in this sector are executed and will modify the sector contents. (Default value).

1. Valid only for sector 0 and sector 15 (the value ‘0’ is returned for other sectors).

Figure 13. Read Lock Register (RDLR) instruction sequence and data-out Sequence



6.8 Page Write (PW)

The Page Write (PW) instruction allows Bytes to be written in the memory. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Page Write (PW) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, three address Bytes and at least one data Byte on Serial Data Input (D). The rest of the page remains unchanged if no power failure occurs during this write cycle.

The Page Write (PW) instruction performs a page erase cycle even if only one Byte is updated.

If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data exceeding the addressed page boundary roll over, and are written from the start address of the same page (the one whose 8 least significant address bits (A7-A0) are all zero). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in *Figure 14*.

If more than 256 Bytes are sent to the device, previously latched data are discarded and the last 256 data Bytes are guaranteed to be written correctly within the same page. If less than 256 Data Bytes are sent to device, they are correctly written at the requested addresses without having any effects on the other Bytes of the same page.

For optimized timings, it is recommended to use the Page Write (PW) instruction to write all consecutive targeted Bytes in a single sequence versus using several Page Write (PW) sequences with each containing only a few Bytes.

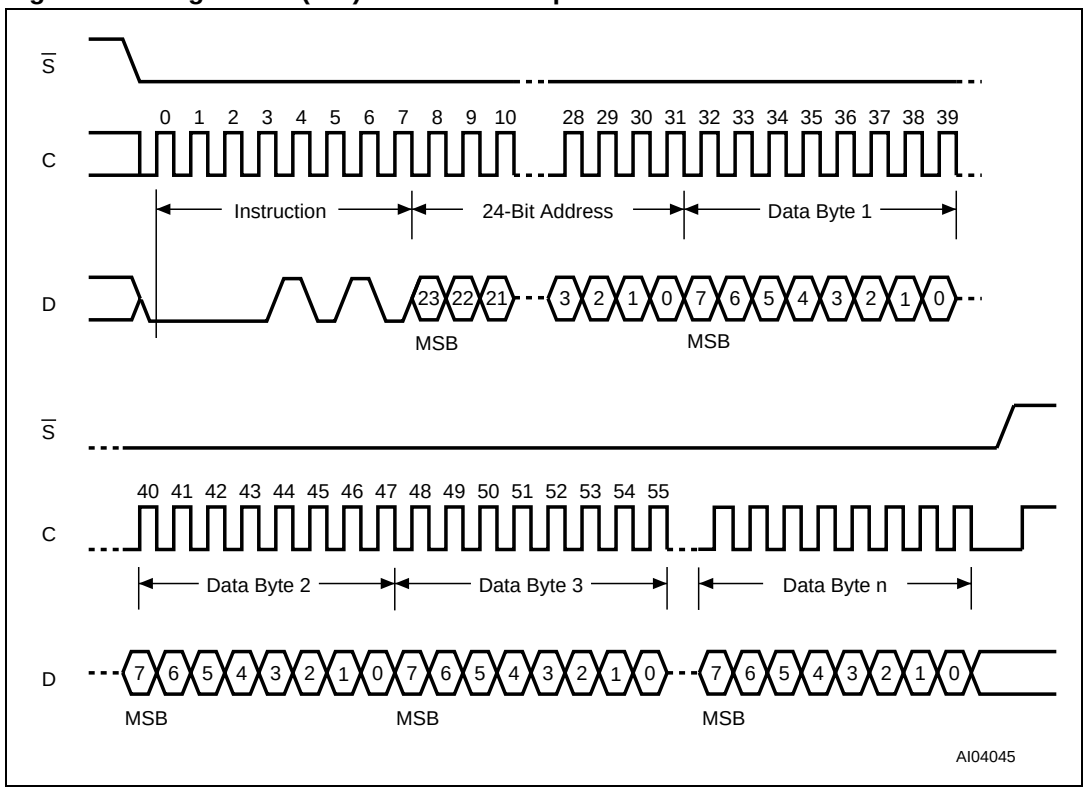
Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last data Byte has been latched in, otherwise the Page Write (PW) instruction is not executed.

As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Page Write cycle (whose duration is t_{PW}) is initiated. While the Page Write cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Write cycle, and is 0 when it is completed. At some unspecified time before the cycle is complete, the Write Enable Latch (WEL) bit is reset.

A Page Write (PW) instruction applied to a page that is Hardware or Software Protected is not executed.

Any Page Write (PW) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 14. Page Write (PW) instruction sequence



1. Address bits A23 to A20 are Don't Care
2. $1 \leq n \leq 256$

6.9 Page Program (PP)

The Page Program (PP) instruction allows Bytes to be programmed in the memory (changing bits from 1 to 0, only). Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Page Program (PP) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, three address Bytes and at least one data Byte on Serial Data Input (D). If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data exceeding the addressed page boundary roll over, and are programmed from the start address of the same page (the one whose 8 least significant address bits (A7-A0) are all zero). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in *Figure 15*.

If more than 256 Bytes are sent to the device, previously latched data are discarded and the last 256 data Bytes are guaranteed to be programmed correctly within the same page. If less than 256 Data Bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other Bytes of the same page.

For optimized timings, it is recommended to use the Page Program (PP) instruction to program all consecutive targeted Bytes in a single sequence versus using several Page Program (PP) sequences with each containing only a few Bytes (see ***Table 16: AC Characteristics***).

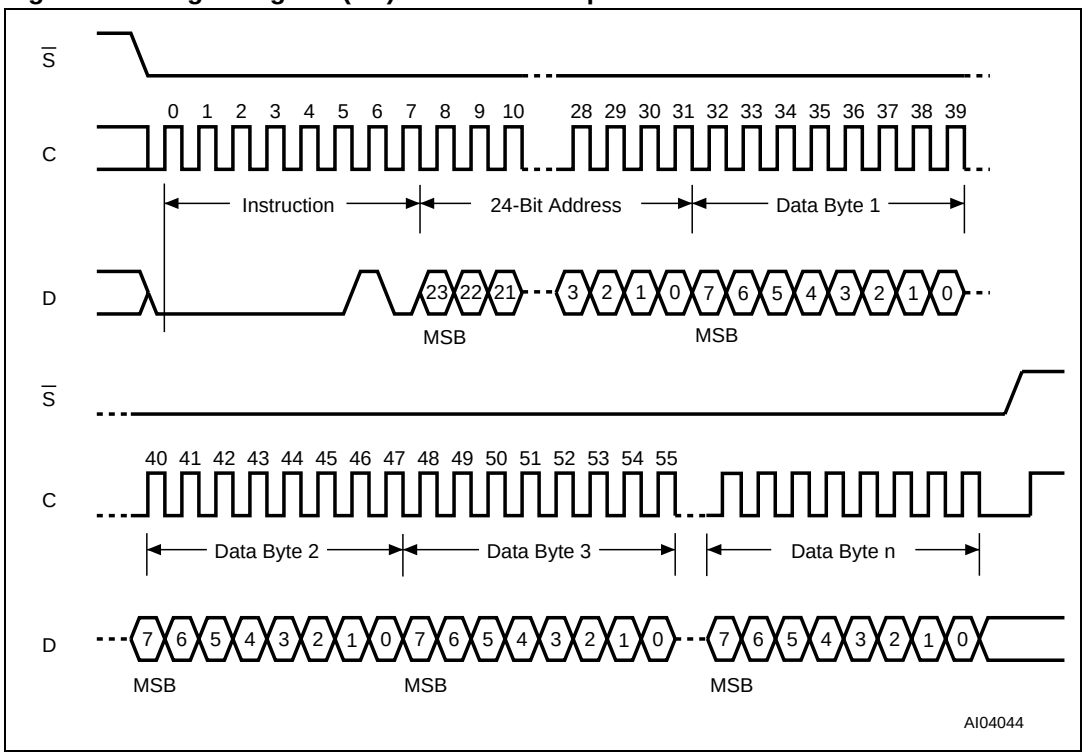
Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last data Byte has been latched in, otherwise the Page Program (PP) instruction is not executed.

As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is complete, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) instruction applied to a page that is Hardware or software Protected is not executed.

Any Page Program (PP) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 15. Page Program (PP) instruction sequence



1. Address bits A23 to A20 are Don't Care
2. $1 \leq n \leq 256$

6.10 Write to Lock Register (WRLR)

The Write to Lock Register (WRLR) instruction allows bits to be changed in the Lock Registers. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Write to Lock Register (WRLR) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, three address Bytes (pointing to any address in the targeted sector/sub-sector) and one data Byte on Serial Data Input (D).

The instruction sequence is shown in *Figure 16*.

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the data Byte has been latched in, otherwise the Write to Lock Register (WRLR) instruction is not executed.

When the Write to Lock Register (WRLR) instruction has been successfully executed, the Write Enable Latch (WEL) bit is reset after a delay time less than t_{SHSL} minimum value.

Any Write to Lock Register (WRLR) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 16. Write to Lock Register (WRLR) instruction sequence

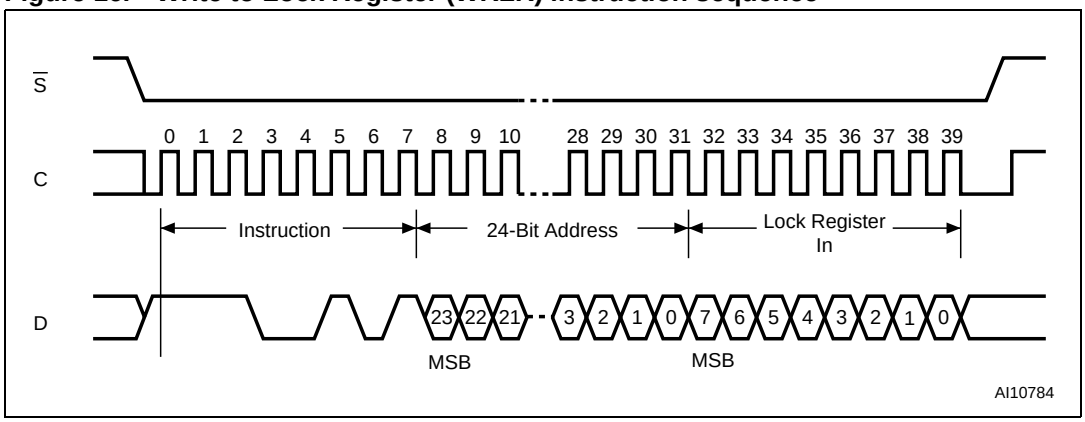


Table 9. Lock Register In

Sector	Bit	Value	
All Sectors Except for Sector 0 and Sector 15	b7-b2	‘0’	
	b1	Sector Lock Down Bit Value (refer to *Table 8*)	
	b0	Sector Write Lock Bit Value (refer to *Table 8*)	
Sector 0 Sector 15	b7	‘1’	Only b3 and b2 are taken into account to modify the sub-sector Write Lock and Lock Down bits(1)
		‘0’	Only b1 and b0 are taken into account to modify the sector Write Lock and Lock Down bits(2)
	b3	Sub-sector Lock Down Bit value (refer to *Table 8*)	
	b2	Sub-sector Write Lock Bit Value (refer to *Table 8*)	
	b1	Sector Lock Down Bit Value (refer to *Table 8*)	
	b0	Sector Write Lock Bit Value (refer to *Table 8*)	

1. b6-b4 and b1-b0 must be reset to ‘0’.
2. b6-b2 must be reset to ‘0’.

Protection always prevails:

- When the Lock Down Bit of Sector 0 or Sector 15 is set to ‘1’.
  - If the Lock Down Bit of Sector 0 is ‘1’, all the Lock Down Bits of the sub-sectors in Sector 0 are forced to ‘1’.
  - If the Lock Down Bit of Sector 15 is ‘1’, all the Lock Down Bits of the sub-sectors in Sector 15 are forced to ‘1’
- When the Write Lock Bit of Sector 0 or Sector 15 is set to ‘1’.
  - if the Write Lock Bit of Sector 0 is ‘1’, the Write Lock Bits of all the sub-sectors in Sector 0 are forced to ‘1’ (even if their Lock Down Bits are set to ‘1’).
  - if the Write Lock Bit of Sector 15 is ‘1’, the Write Lock Bits of all the sub-sectors in Sector 15 are forced to ‘1’ (even if their Lock Down Bits are set to ‘1’).
- When the Write Lock Bit of Sector 0 or Sector 15 is reset to ‘0’.
  - if the Write Lock Bit of Sector 0 is ‘0’, all the sub-sectors in Sector 0 whose Lock Down Bit is ‘0’ have their Write Lock Bits forced to ‘0’.
  - if the Write Lock Bit of Sector 15 is ‘0’, all the sub-sectors in Sector 15 whose Lock Down Bit is ‘0’ have their Write Lock Bits forced to ‘0’.
- When the Write Lock Bit of any sector or sub-sector is set to ‘1’, any instruction that may modify the contents of this sector or sub-sector will be rejected (including Sector Erase and Bulk Erase).

Note that when the WRLR instruction acts both on Write Lock (WL) and Lock Down (LD) bits, it firstly programs the WL bit, and then the LD bit.

As an example, if a sub-sector Lock Register settings are xxxx0101b and a WRLR instruction is issued with a Lock Register In data set to 00000010b:

1. the sector WL bit is first set to ‘0’ (and all sub-sectors that are not locked-down will have their WL bit reset to ‘0’).
2. the sector LD bit and all sub-sectors LD bits are set to ‘1’.

In this case, the final value of the above sub-sector Lock Register is xxxx1010b.

6.11 Page Erase (PE)

The Page Erase (PE) instruction sets to 1 (FFh) all bits inside the chosen page. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Page Erase (PE) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, and three address Bytes on Serial Data Input (D). Any address inside the Page is a valid address for the Page Erase (PE) instruction. Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

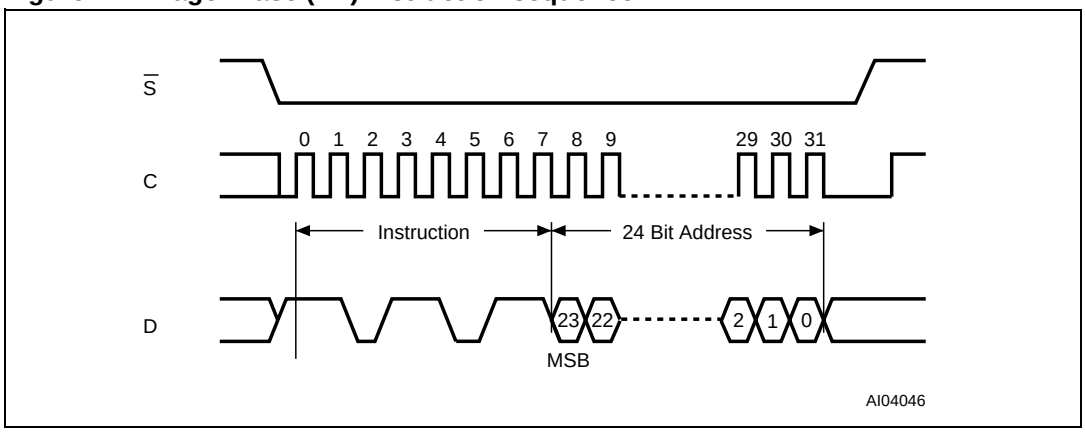
The instruction sequence is shown in *Figure 17*.

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last address Byte has been latched in, otherwise the Page Erase (PE) instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Page Erase cycle (whose duration is t_{PE}) is initiated. While the Page Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is complete, the Write Enable Latch (WEL) bit is reset.

A Page Erase (PE) instruction applied to a page that is Hardware or software Protected is not executed.

Any Page Erase (PE) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 17. Page Erase (PE) instruction sequence



1. Address bits A23 to A20 are Don't Care.

6.12 Sector Erase (SE)

The Sector Erase (SE) instruction sets to 1 (FFh) all bits inside the chosen sector. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Sector Erase (SE) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, and three address Bytes on Serial Data Input (D). Any address inside the Sector (see *Table 4*) is a valid address for the Sector Erase (SE) instruction. Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

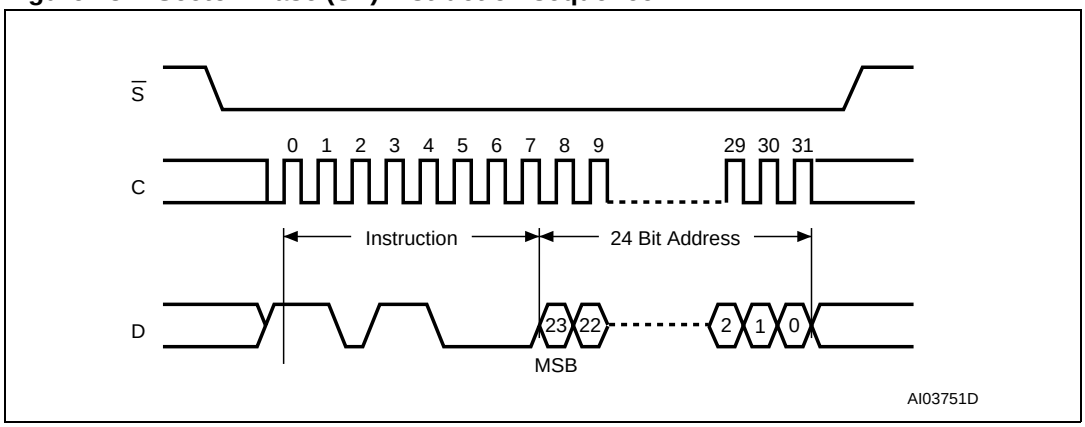
The instruction sequence is shown in *Figure 18*.

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last address Byte has been latched in, otherwise the Sector Erase (SE) instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Sector Erase cycle (whose duration is t_{SE}) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is complete, the Write Enable Latch (WEL) bit is reset.

A Sector Erase (SE) instruction applied to a sector that contains a page that is Hardware or software Protected is not executed.

Any Sector Erase (SE) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 18. Sector Erase (SE) instruction sequence



1. Address bits A23 to A20 are Don't Care.

6.13 Bulk Erase (BE)

The Bulk Erase (BE) instruction sets all bits to 1 (FFh). Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

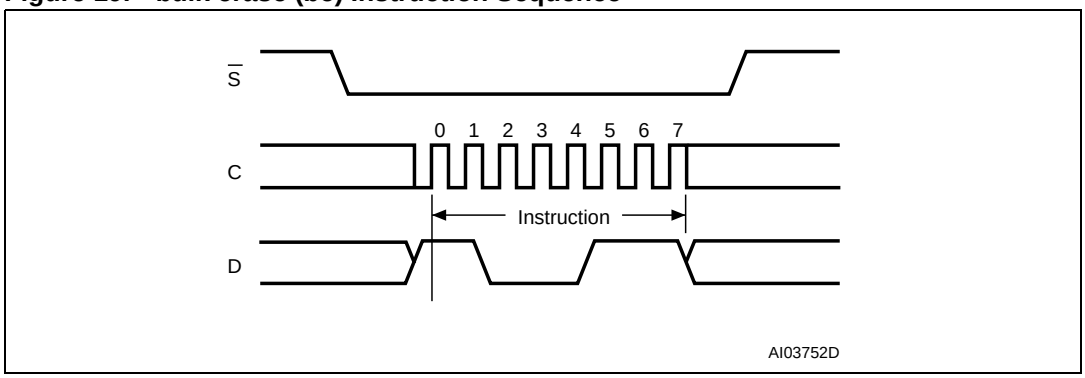
The Bulk Erase (BE) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code on Serial Data Input (D). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in *Figure 19*.

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Bulk Erase instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Bulk Erase cycle (whose duration is t_{BE}) is initiated. While the Bulk Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Bulk Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

Any Bulk Erase (BE) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress. A Bulk Erase (BE) instruction is ignored if at least one sector or sub-sector is write-protected (Hardware or Software protection).

Figure 19. bulk erase (be) Instruction Sequence



6.14 Deep Power-down (DP)

Executing the Deep Power-down (DP) instruction is the only way to put the device in the lowest consumption mode (the Deep Power-down mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase instructions.

Driving Chip Select ($\overline{S}$) High deselects the device, and puts the device in the Standby mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-down mode. The Deep Power-down mode can only be entered by executing the Deep Power-down (DP) instruction, subsequently reducing the standby current (from I_{CC1} to I_{CC2}, as specified in *Table 15*).

Once the device has entered the Deep Power-down mode, all instructions are ignored except the Release from Deep Power-down (RDP) instruction. Issuing the Release from Deep Power-down (RDP) instruction will cause the device to exit the Deep Power-down mode.

The Deep Power-down mode automatically stops at Power-down, and the device always Powers-up in the Standby mode.

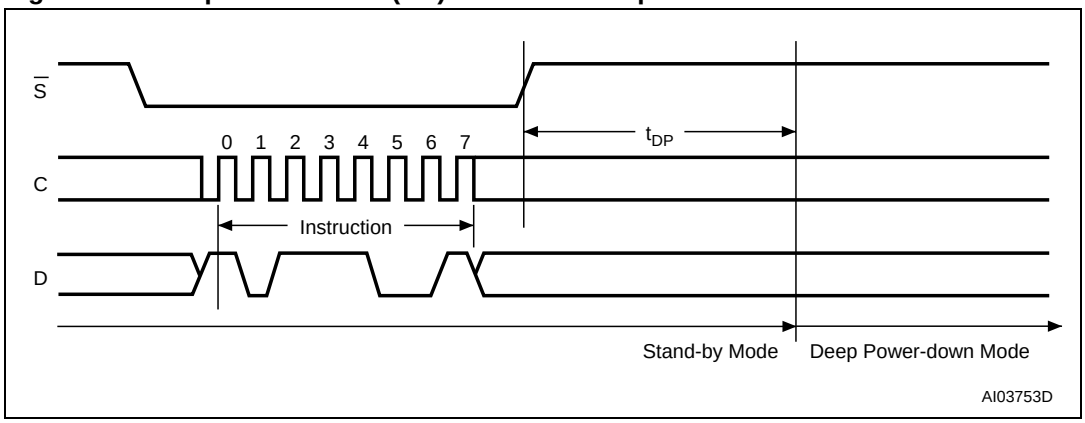
The Deep Power-down (DP) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code on Serial Data Input (D). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in *Figure 20*.

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Deep Power-down (DP) instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, it requires a delay of t_{DP} before the supply current is reduced to I_{CC2} and the Deep Power-down mode is entered.

Any Deep Power-down (DP) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 20. Deep Power-down (DP) instruction sequence



6.15 Release from Deep Power-down (RDP)

Once the device has entered the Deep Power-down mode, all instructions are ignored except the Release from Deep Power-down (RDP) instruction. Executing this instruction takes the device out of the Deep Power-down mode.

The Release from Deep Power-down (RDP) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code on Serial Data Input (D). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

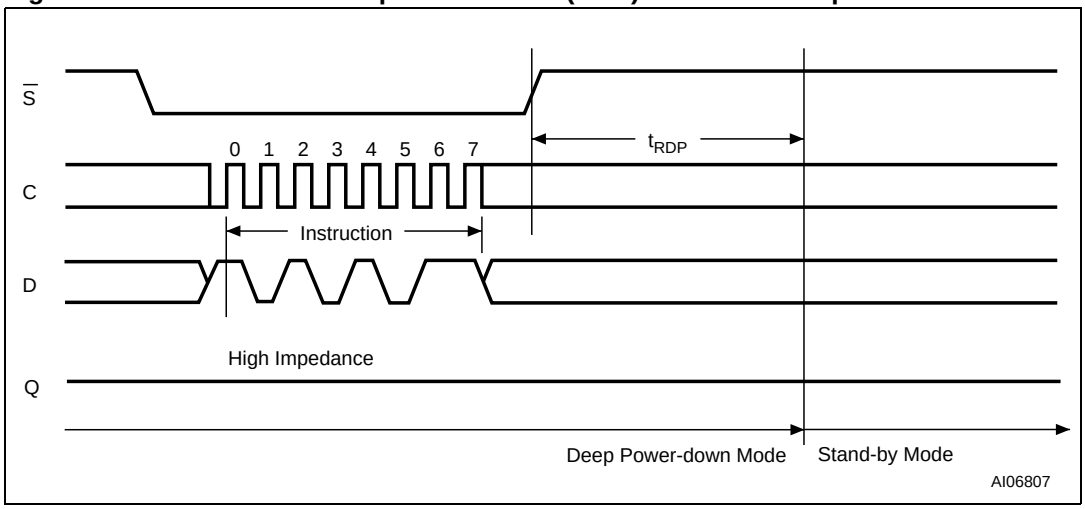
The instruction sequence is shown in *Figure 21*.

The Release from Deep Power-down (RDP) instruction is terminated by driving Chip Select ($\overline{S}$) High. Sending additional clock cycles on Serial Clock (C), while Chip Select ($\overline{S}$) is driven Low, cause the instruction to be rejected, and not executed.

After Chip Select ($\overline{S}$) has been driven High, followed by a delay, t_{RDP}, the device is put in the Standby mode. Chip Select ($\overline{S}$) must remain High at least until this period is over. The device waits to be selected, so that it can receive, decode and execute instructions.

Any Release from Deep Power-down (RDP) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 21. Release from Deep Power-down (RDP) instruction sequence



7 Power-up and Power-down

At Power-up and Power-down, the device must not be selected (that is Chip Select ($\overline{S}$) must follow the voltage applied on V_{CC}) until V_{CC} reaches the correct value:

- V_{CC}(min) at Power-up, and then for a further delay of t_{VSL}
- V_{SS} at Power-down

Usually a simple pull-up resistor on Chip Select ($\overline{S}$) can be used to ensure safe and proper Power-up and Power-down.

To avoid data corruption and inadvertent write operations during power-up, a Power On Reset (POR) circuit is included. The logic inside the device is held reset while V_{CC} is less than the Power On Reset (POR) threshold voltage, V_{WI} – all operations are disabled, and the device does not respond to any instruction.

Moreover, the device ignores all Write Enable (WREN), Page Write (PW), Page Program (PP), Page Erase (PE), Sector Erase (SE), Bulk Erase (BE) and Write to Lock Register (WRLR) instructions until a time delay of t_{PUW} has elapsed after the moment that V_{CC} rises above the V_{WI} threshold. However, the correct operation of the device is not guaranteed if, by this time, V_{CC} is still below V_{CC}(min). No Write, Program or Erase instructions should be sent until the later of:

- t_{PUW} after V_{CC} passed the V_{WI} threshold
- t_{VSL} after V_{CC} passed the V_{CC}(min) level

These values are specified in *Table 10*.

If the delay, t_{VSL}, has elapsed, after V_{CC} has risen above V_{CC}(min), the device can be selected for READ instructions even if the t_{PUW} delay is not yet fully elapsed.

As an extra protection, the Reset ($\overline{Reset}$) signal could be driven Low for the whole duration of the Power-up and Power-down phases.

At Power-up, the device is in the following state:

- The device is in the Standby mode (not the Deep Power-down mode).
- The Write Enable Latch (WEL) bit is reset.

Normal precautions must be taken for supply rail decoupling, to stabilize the V_{CC} supply. Each device in a system should have the V_{CC} rail decoupled by a suitable capacitor close to the package pins. (Generally, this capacitor is of the order of 0.1µF).

At Power-down, when V_{CC} drops from the operating voltage, to below the Power On Reset (POR) threshold voltage, V_{WI}, all operations are disabled and the device does not respond to any instruction. (The designer needs to be aware that if a Power-down occurs while a Write, Program or Erase cycle is in progress, some data corruption can result.)

Figure 22. Power-up timing

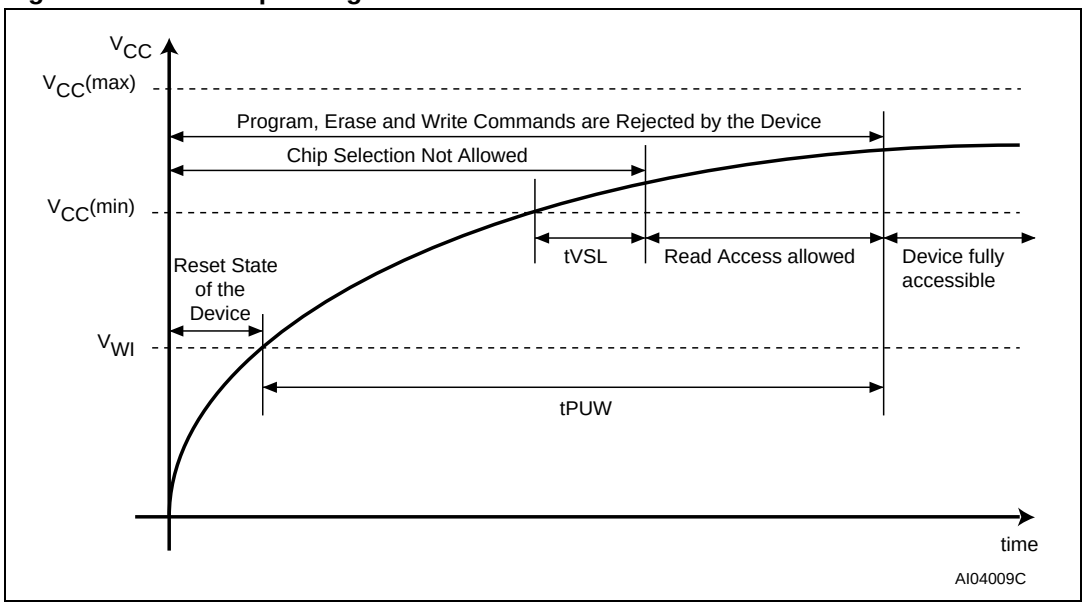


Table 10. Power-Up timing and V_{WI} threshold

Symbol	Parameter	Min.	Max.	Unit
t_{VSL}(1)	V_{CC}(min) to $\overline{S}$ low	30		µs
t_{PUW}(1)	Time delay before the first Write, Program or Erase instruction	1	10	ms
V_{WI}(1)	Write Inhibit Voltage	1.5	2.5	V

1. These parameters are characterized only, over the temperature range –40°C to +85°C.

8 Initial delivery state

The device is delivered with the memory array erased: all bits are set to 1 (each Byte contains FFh). All usable Status Register bits are 0.

9 Maximum rating

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 11. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_{STG}	Storage Temperature	–65	150	°C
V_{IO}	Input and Output Voltage (with respect to Ground)	–0.6	4.0	V
V_{CC}	Supply Voltage	–0.6	4.0	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model)(1)	–2000	2000	V

1. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 Ω, R2=500 Ω).

10 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 12. Operating conditions

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	2.7	3.6	V
T_A	Ambient Operating Temperature	–40	85	°C

Table 13. AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load Capacitance	30		pF
	Input Rise and Fall Times		5	ns
	Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$		V
	Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$		V

1. Output Hi-Z is defined as the point where data out is no longer driven.

Figure 23. AC measurement I/O waveform

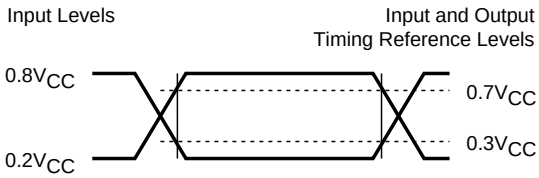


Table 14. Capacitance

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C_{OUT}	Output Capacitance (Q)	V_{OUT} = 0V		8	pF
C_{IN}	Input Capacitance (other pins)	V_{IN} = 0V		6	pF

1. Sampled only, not 100% tested, at T_A=25°C and a frequency of 20 MHz.

Table 15. DC Characteristics

Symbol	Parameter	Test Condition (in addition to those in *Table 12*)	Min.	Max.	Unit
I_{LI}	Input Leakage Current			± 2	µA
I_{LO}	Output Leakage Current			± 2	µA
I_{CC1}	Standby Current (Standby and Reset modes)	$\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}		50	µA
I_{CC2}	Deep Power-down Current	$\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}		10	µA
I_{CC3}	Operating Current (FAST_READ)	C = 0.1V_{CC} / 0.9.V_{CC} at 50MHz, Q = open		8	mA
I_{CC4}	Operating Current (PW)	$\overline{S} = V_{CC}$		15	mA
I_{CC5}	Operating Current (SE)	$\overline{S} = V_{CC}$		15	mA
V_{IL}	Input Low Voltage		– 0.5	0.3V_{CC}	V
V_{IH}	Input High Voltage		0.7V_{CC}	V_{CC}+0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –100µA	V_{CC}–0.2		V

Table 16. AC Characteristics

Test conditions specified in *Table 12* and *Table 13*						
Symbol	**Alt.**	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
f_C	f_C	Clock Frequency for the following instructions: FAST_READ, RDLR, PW, PP, WRLR, PE, SE, DP, RDP, WREN, WRDI, RDSR	D.C.		50	MHz
f_R		Clock Frequency for READ instructions	D.C.		20	MHz
t_{CH} (1)	t_{CLH}	Clock High Time	9			ns
t_{CL} (1)	t_{CLL}	Clock Low Time	9			ns
		Clock Slew Rate (2) (peak to peak)	0.1			V/ns
t_{SLCH}	t_{CSS}	$\overline{S}$ Active Setup Time (relative to C)	5			ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time (relative to C)	5			ns
t_{DVCH}	t_{DSU}	Data In Setup Time	2			ns
t_{CHDX}	t_{DH}	Data In Hold Time	5			ns
t_{CHSH}		$\overline{S}$ Active Hold Time (relative to C)	5			ns
t_{SHCH}		$\overline{S}$ Not Active Setup Time (relative to C)	5			ns
t_{SHSL}	t_{CSH}	$\overline{S}$ Deselect Time	100			ns
t_{SHQZ} (2)	t_{DIS}	Output Disable Time			8	ns
t_{CLQV}	t_V	Clock Low to Output Valid			8	ns
t_{CLQX}	t_{HO}	Output Hold Time	0			ns
t_{THSL}		Top Sector Lock Setup Time	50			ns
t_{SHTL}		Top Sector Lock Hold Time	100			ns
t_{DP} (2)		$\overline{S}$ to Deep Power-down			3	µs
t_{RDP} (2)		$\overline{S}$ High to Standby Mode			30	µs
t_{PW} (3)		Page Write Cycle Time (256 Bytes)		11	25	ms
		Page Write Cycle Time (n Bytes)		10.1 + n * 0.9/256		
t_{PP} (3)		Page Program Cycle Time (256 Bytes)		1.35	5	ms
		Page Program Cycle Time (n Bytes)		0.45 + n * 0.9/256		
t_{PE}		Page Erase Cycle Time		10	20	ms
t_{SE}		Sector Erase Cycle Time		1	5	s
t_{BE}		Bulk Erase Cycle Time		10	60	s

1. $t_{CH} + t_{CL}$ must be greater than or equal to $1/ f_C$
2. Value guaranteed by characterization, not 100% tested in production.
3. When using PP and PW instructions to update consecutive Bytes, optimized timings are obtained with one sequence including all the Bytes versus several sequences of only a few Bytes ($1 \leq n \leq 256$).

Figure 24. Serial input timing

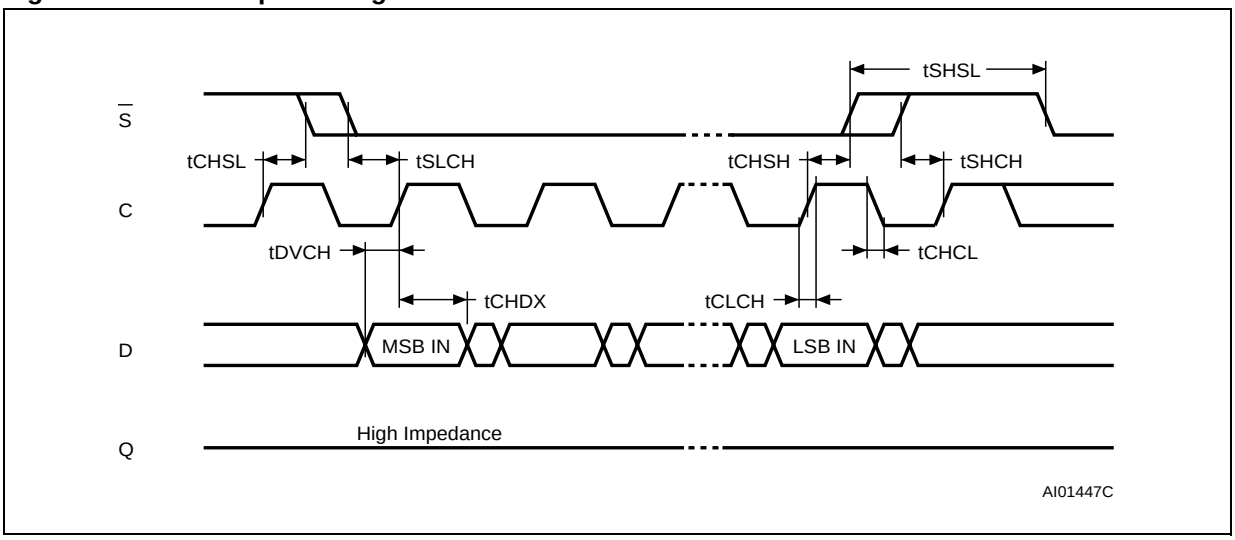


Figure 25. Top Sector Lock setup and hold timing

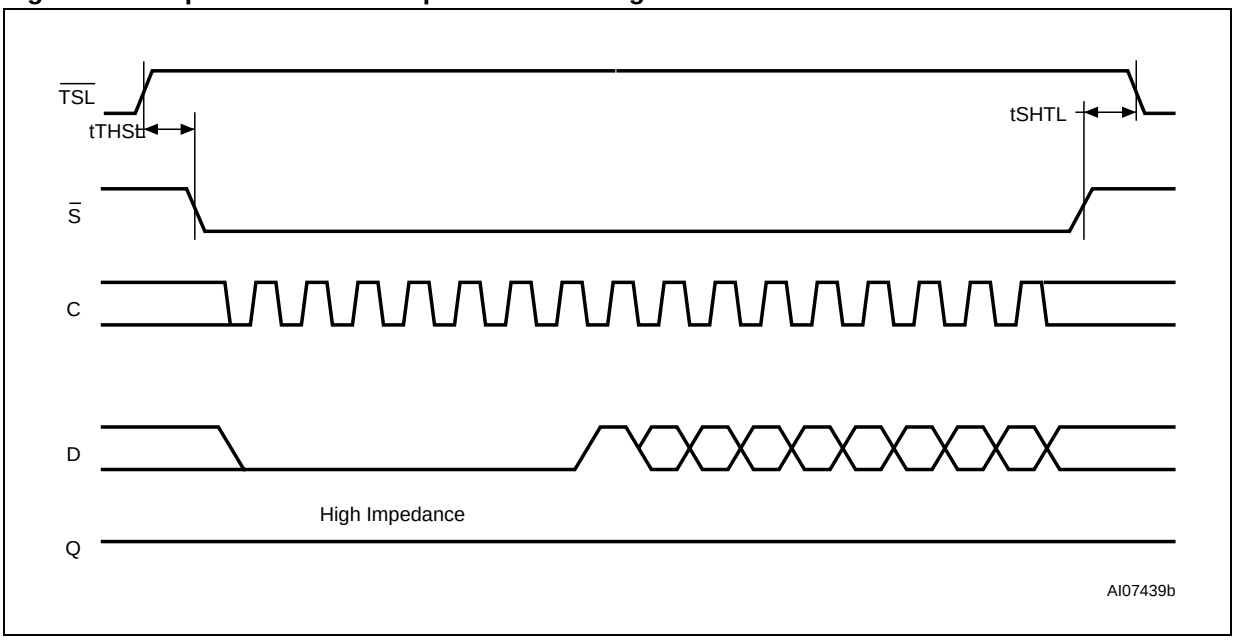


Figure 26. Output Timing

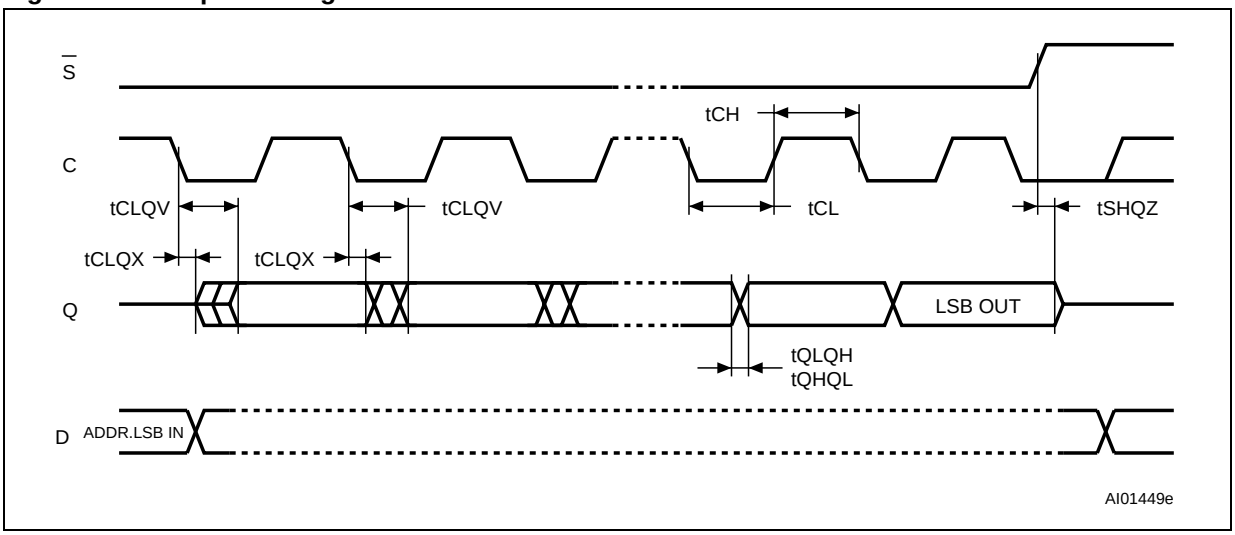
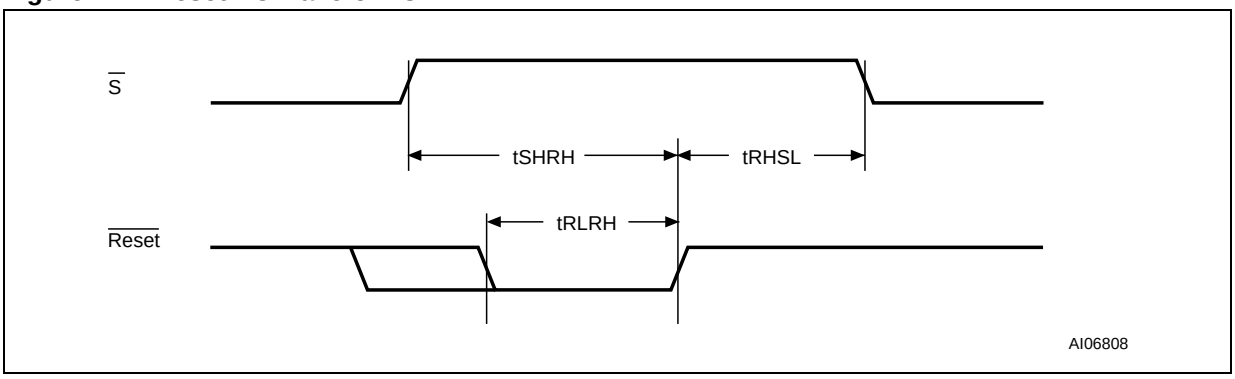


Table 17. Reset timings

Test conditions specified in *Table 12* and *Table 13*							
Symbol	**Alt.**	**Parameter**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
t_{RLRH}(1)	t_{RST}	Reset Pulse Width		10			µs
t_{RHSL}	t_{REC}	Reset Recovery Time	after any operation except for PW, PP, PE, SE and BE			30	µs
			After PW, PP, PE, SE and BE operations(1)			300	µs
t_{SHRH}		Chip Select High to Reset High	Chip should have been deselected before Reset is de-asserted	10			ns

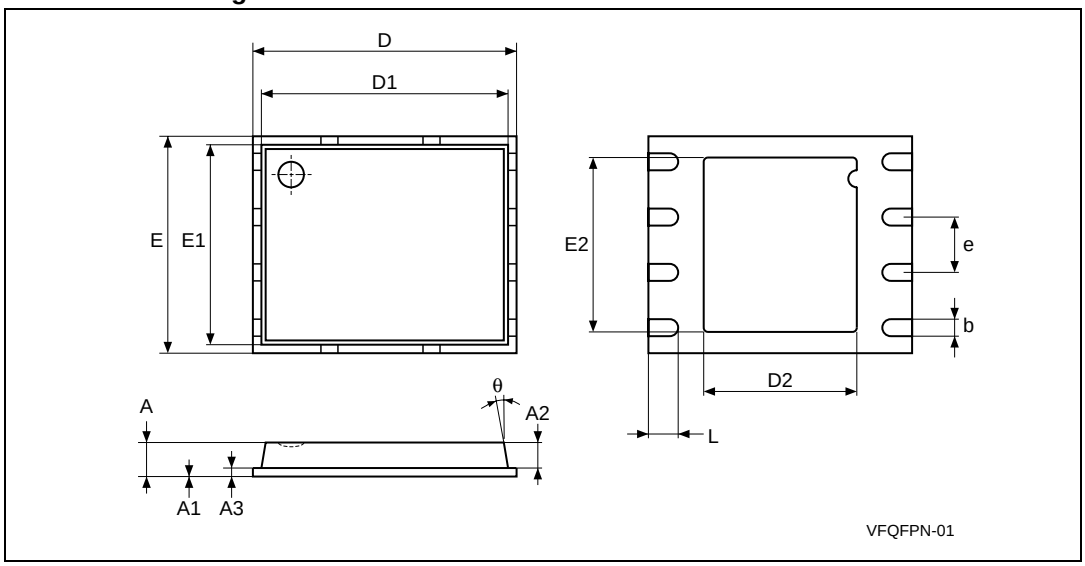
1. Value guaranteed by characterization, not 100% tested in production.

Figure 27. Reset AC waveforms



11 Package mechanical

Figure 28. VFQFPN8 (MLP8) 8-lead Very thin Dual Flat Package No lead, 6x5mm, Package Outline

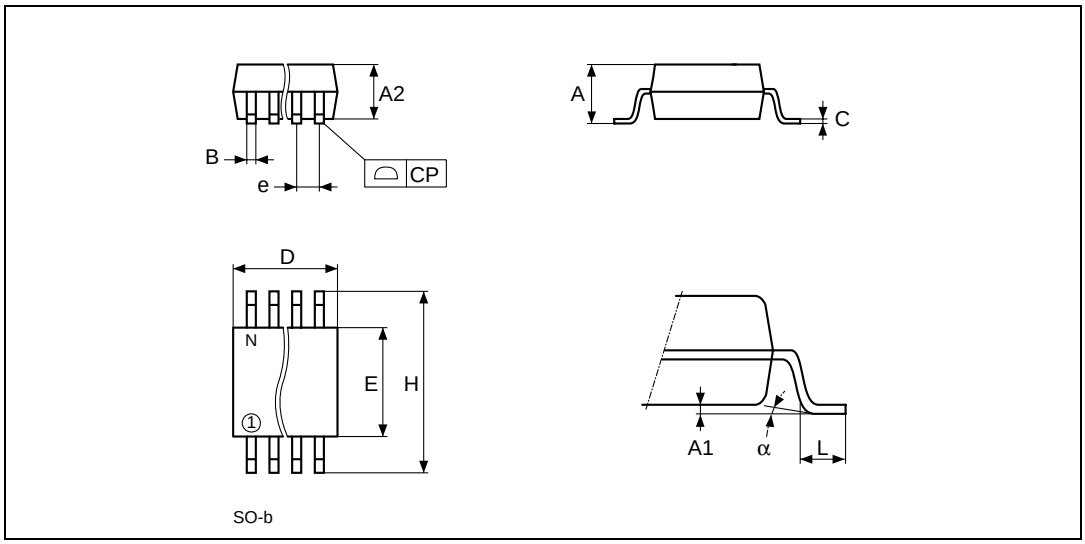


1. Drawing is not to scale.
2. The circle in the top view of the package indicates the position of pin 1.

Table 18. VFQFPN8 (MLP8) 8-lead Very thin Dual Flat Package No lead, 6x5mm, Package Mechanical Data

Symbol	millimeters			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	0.85		1.00	0.0335		0.0394
A1		0.00	0.05		0.0000	0.0020
A2	0.65			0.0256		
A3	0.20			0.0079		
b	0.40	0.35	0.48	0.0157	0.0138	0.0189
D	6.00			0.2362		
D1	5.75			0.2264		
D2	3.40	3.20	3.60	0.1339	0.1260	0.1417
E	5.00			0.1969		
E1	4.75			0.1870		
E2	4.00	3.80	4.20	0.1575	0.1496	0.1654
e	1.27			0.0500		
L	0.60	0.50	0.75	0.0236	0.0197	0.0295
θ			12°			12°

Figure 29. SO8 wide – 8 lead Plastic Small Outline, 208 mils body width, Package Outline



1. Drawing is not to scale.
2. The circle in the top view of the package indicates the position of pin 1.

Table 19. SO8 wide – 8 lead Plastic Small Outline, 208 mils body width, mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			2.03			0.080
A1		0.10	0.25		0.004	0.010
A2			1.78			0.070
B		0.35	0.45		0.014	0.018
C	0.20	–	–	0.008	–	–
CP			0.10			0.004
D		5.15	5.35		0.203	0.211
E		5.20	5.40		0.205	0.213
e	1.27	–	–	0.050	–	–
H		7.70	8.10		0.303	0.319
L		0.50	0.80		0.020	0.031
α		0°	10°		0°	10°
N	8			8		

12 Part numbering

Table 20. Ordering information scheme

Example: M25PE80 – V MP 6 T P

Device Type

M25PE = Page-Erasable Serial Flash Memory

Device Function

80 = 8Mbit (1Mb x 8)

Operating Voltage

V = V_{CC} = 2.7 to 3.6V

Package

MW = SO8 (208 mils width)

MP = VFQFPN8 6x5mm (MLP8)

Device Grade

6 = Industrial: device tested with standard test flow over –40 to 85 °C

Option

blank = Standard Packing

T = Tape and Reel Packing

Plating Technology

P or G = ECOPACK® (RoHs compliant)

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office.

The category of Second-Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

13 Revision history

Table 21. Document revision history

Date	Version	Changes
24-Nov-2004	0.1	First Issue.
07-Dec-2004	0.2	4KB Software protection granularity extended to Sector 15.
10-May-2005	0.3	SO16W package removed, SO8W package added. End timing line of t_{SHQZ} modified in *Figure 26: Output Timing*. Plating Technology options modified in *Table 20: Ordering information scheme*. Minor text changes. Tables *2* and *3* and *Figure 5* for details on the software protection scheme.
25-Jul-2005	0.4	Lock Register programming sequence detailed in Section *Write to Lock Register (WRLR)*. Sections *An easy way to modify data*, *A fast way to modify data*, *Page Write (PW)* and *Page Program (PP)*, updated to explain when using Page Write and Page Program instructions. Bulk Erase cycle time (t_{BE}), Page Write cycle time (t_{PW}) and Page Program cycle time (t_{PP}) updated in *Table 16: AC Characteristics*.
24-Aug-2005	1.0	Version number updated for internet. No document changes.
25-Aug-2005	2.0	Document status updated to Preliminary Data.
22-Nov-2005	3.0	Page Program cycle time, t_{PP}, and Page Write Cycle Time (n Bytes), t_{PW}, updated in *Table 16: AC Characteristics*. I_{CC3} modified in *Table 15: DC Characteristics*. t_{SLCH}, t_{CHSL}, t_{CHSH}, t_{SHCH} and t_{BE} modified in *Table 16: AC Characteristics*. MLP package renamed. Under *Plating Technology*, Blank option removed. *Note 3* to *Table 16* modified. Address modified in *Figure 6: Block Diagram*. Note added to *Figure 28* and *Figure 29*. Document status promoted from Preliminary Data to full Datasheet status.
12-May-2006	4	Don't care address bits modified in *Note 1* (below *Figure 11*) , *Note 1* (below *Figure 12*), *Note 1* (below *Figure 14*) , *Note 1* (below *Figure 15*), *Note 1* (below *Figure 17*) and *Note 1* (below *Figure 18*). Small text changes.

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